MC33171, MC33172, MC33174, NCV33172

Single Supply 3.0 V to 44 V, Low Power Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74 series of monolithic operational amplifiers. These devices operate at 180 μA per amplifier and offer 1.8 MHz of gain bandwidth product and 2.1 V/μs slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential (V_{EE}). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/72/74 are specified over the industrial/automotive temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic as well as the surface mount packages.

Features

- Low Supply Current: 180 μA (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or ±1.5 V to ±22 V
- Wide Input Common Mode Range, Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14.2 V to +14.2 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

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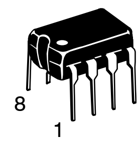
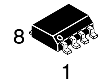


PDIP−8
P SUFFIX
CASE 626



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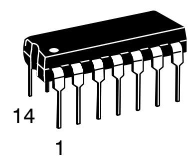
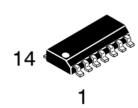
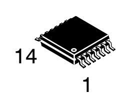
D, VD SUFFIX
CASE 751



PDIP−14
P, VP SUFFIX
CASE 646



SO−14
D, VD SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

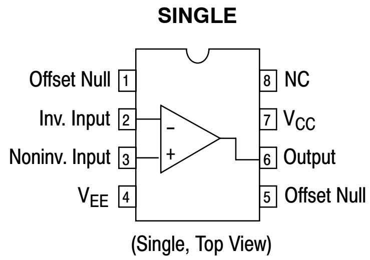
ORDERING INFORMATION

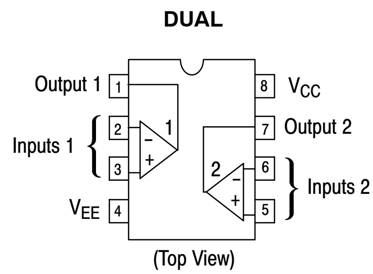
See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

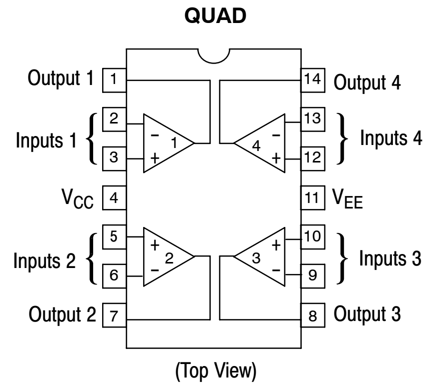
DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

PIN CONNECTIONS







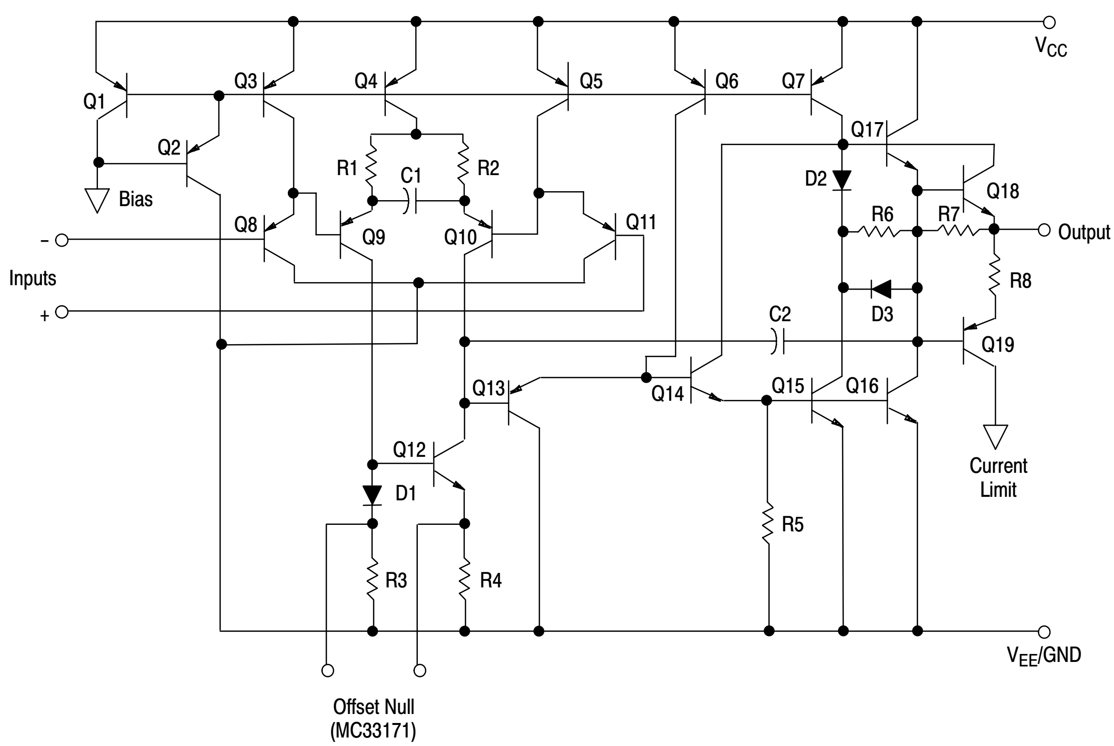


Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±22	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	(Note 3)	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		–	2.0	4.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		–	2.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} (Note 3)		–	–	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	–	10	–	μV/°C
Input Bias Current (V_{CM} = 0 V)	I_{IB}				nA
T_A = +25°C		–	20	100	
T_A = T_{low} to T_{high} (Note 3)		–	–	200	
Input Offset Current (V_{CM} = 0 V)	I_{IO}				nA
T_A = +25°C		–	5.0	20	
T_A = T_{low} to T_{high} (Note 3)		–	–	40	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 k)	A_{VOL}				V/mV
T_A = +25°C		50	500	–	
T_A = T_{low} to T_{high} (Note 3)		25	–	–	
Output Voltage Swing	V_{OH}				V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C		3.5	4.3	–	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.6	14.2	–	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high} (Note 3)		13.3	–	–	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C	V_{OL}	–	0.05	0.15	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		–	−14.2	−13.6	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high} (Note 3)		–	–	−13.3	
Output Short Circuit (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		3.0	5.0	–	
Sink		15	27	–	
Input Common Mode Voltage Range	V_{ICR}				V
T_A = +25°C		V_{EE} to (V_{CC} −1.8)			
T_A = T_{low} to T_{high} (Note 3)		V_{EE} to (V_{CC} −2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k), T_A = +25°C	CMRR	80	90	–	dB
Power Supply Rejection Ratio (R_S = 100 Ω), T_A = +25°C	PSRR	80	100	–	dB
Power Supply Current (Per Amplifier)	I_D				μA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		–	180	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		–	220	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} (Note 3)		–	–	300	

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. MC3317x T_{low} = −40°C T_{high} = +85°C
   MC3317xV, NCV33172 T_{low} = −40°C T_{high} = +125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 k, C_L = 100 pF)	SR				V/μs
A_V +1		1.6	2.1	–	
A_V −1		–	2.1	–	
Gain Bandwidth Product (f = 100 kHz)	GBW	1.4	1.8	–	MHz
Power Bandwidth	BWp				kHz
A_V = +1.0 R_L = 10 k, V_O = 20 V_{pp}, THD = 5%		–	35	–	
Phase Margin	ϕ_m				Deg
R_L = 10 k		–	60	–	
R_L = 10 k, C_L = 100 pF		–	45	–	
Gain Margin	A_m				dB
R_L = 10 k		–	15	–	
R_L = 10 k, C_L = 100 pF		–	5.0	–	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	–	32	–	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	–	0.2	–	pA/$\sqrt{Hz}$
Differential Input Resistance	R_{in}				MΩ
V_{cm} = 0 V		–	300	–	
Input Capacitance	C_{in}	–	0.8	–	pF
Total Harmonic Distortion	THD				%
A_V = +10, R_L = 10 k, 2.0 V_{pp} ≤ V_O ≤ 20 V_{pp}, f = 10 kHz		–	0.03	–	
Channel Separation (f = 10 kHz)	CS	–	120	–	dB
Open Loop Output Impedance (f = 1.0 MHz)	z_o	–	100	–	Ω

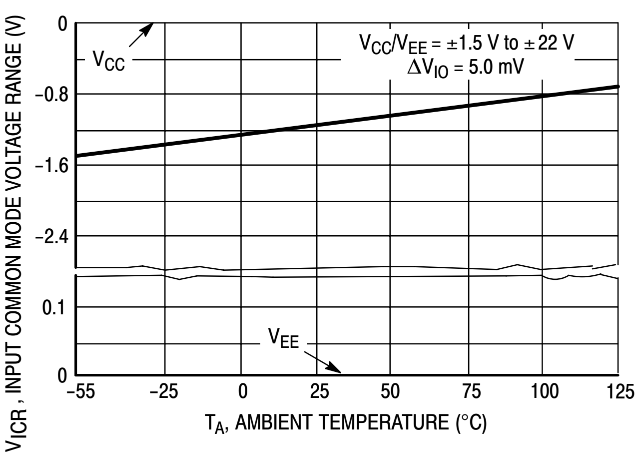


Figure 2. Input Common Mode Voltage Range versus Temperature

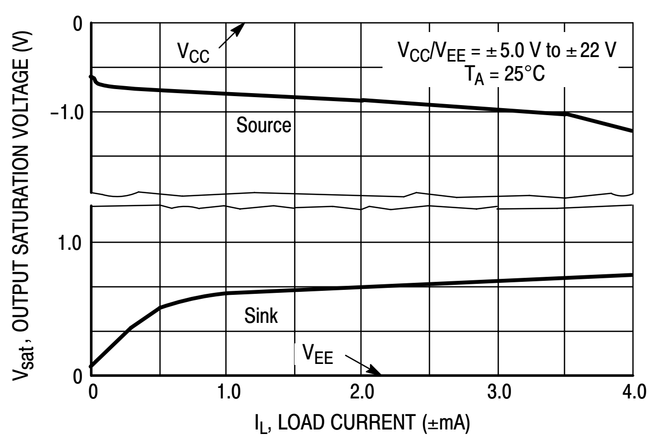


Figure 3. Split Supply Output Saturation versus Load Current

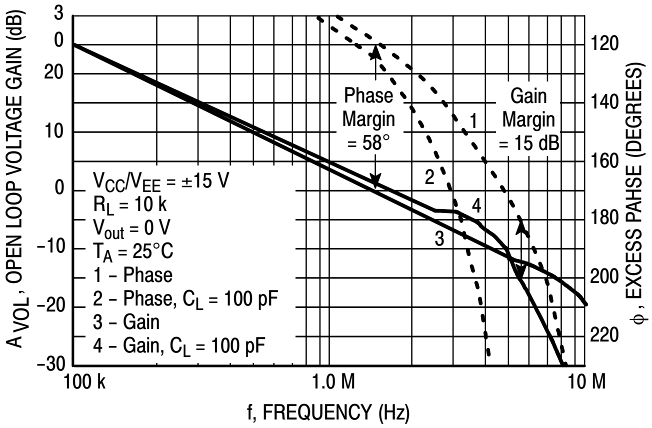


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

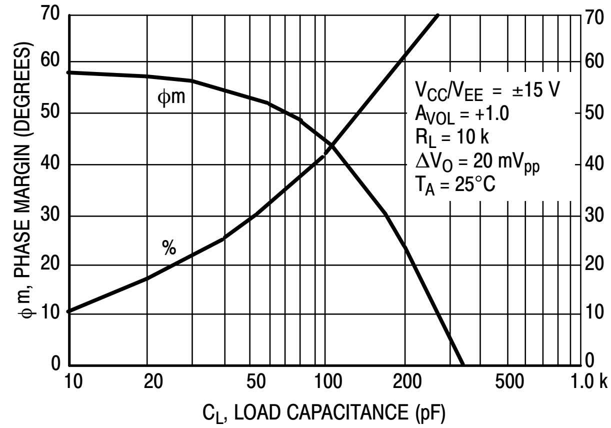


Figure 5. Phase Margin and Percent Overshoot versus Load Capacitance

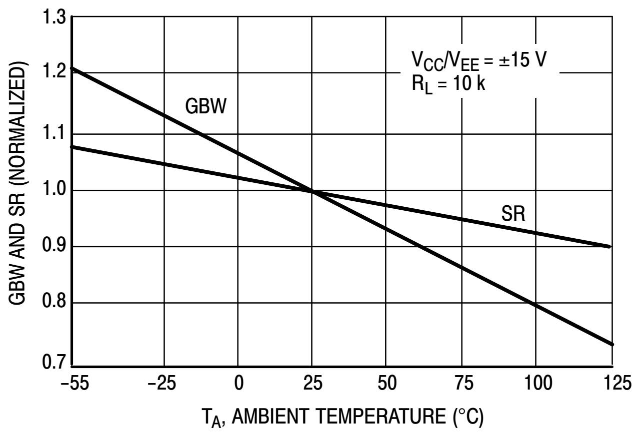


Figure 6. Normalized Gain Bandwidth Product and Slew Rate versus Temperature

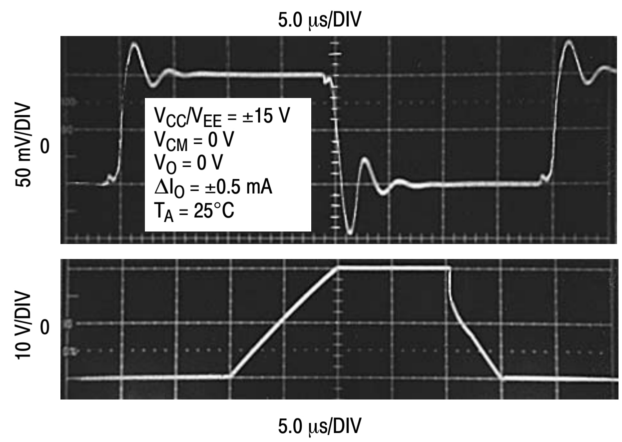


Figure 7. Small and Large Signal Transient Response

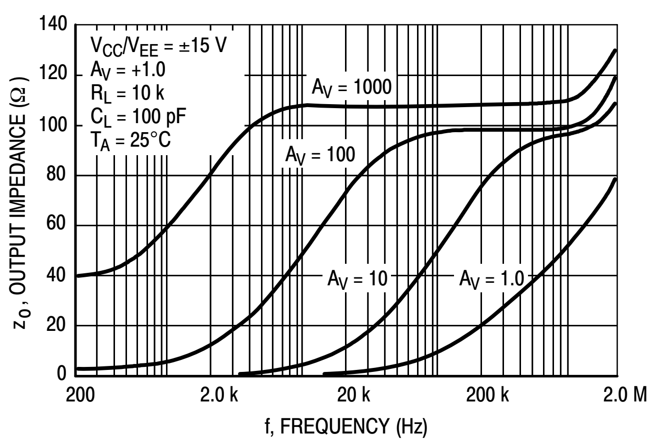


Figure 8. Output Impedance and Frequency

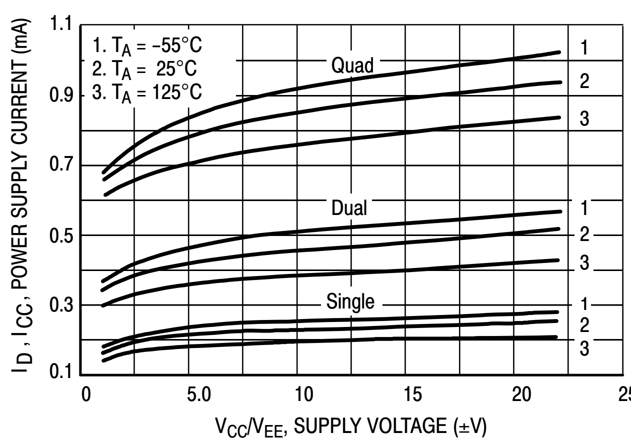


Figure 9. Supply Current versus Supply Voltage

APPLICATIONS INFORMATION – CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D−to−A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 μs, and within 1/2 LSB of 12 bits in 4.8 μs for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ±2.1 V/μs. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 V/μs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 V of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vpp swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull−up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull−down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For sink currents (> 0.4 mA), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE}$ +1.0 V). Therefore an unprecedented peak−to−peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull−up capability.

Because the PNP output emitter−follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The 60° phase margin and 15 dB gain margin, as well as the general gain and phase characteristics, are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 V, these amplifiers are functional to at least 3.0 V @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity, or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

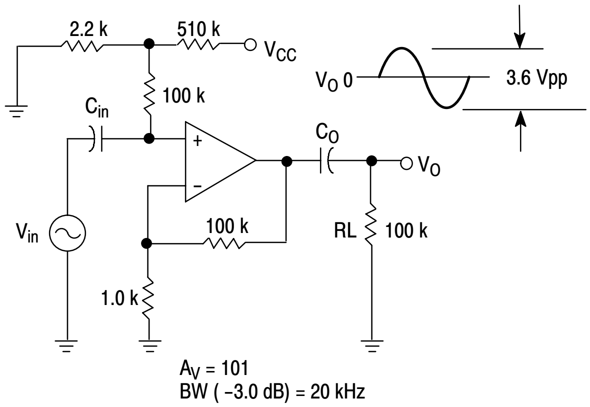


Figure 10. AC Coupled Noninverting Amplifier with Single +5.0 V Supply

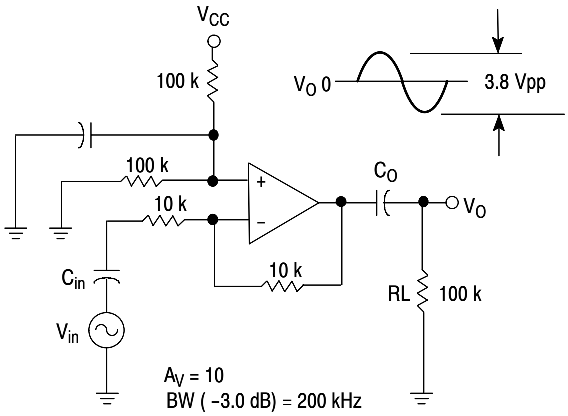


Figure 11. AC Coupled Inverting Amplifier with Single +5.0 V Supply

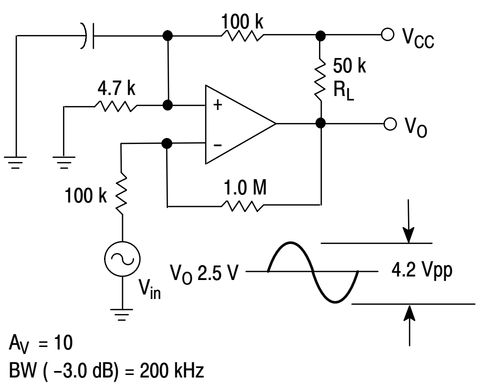
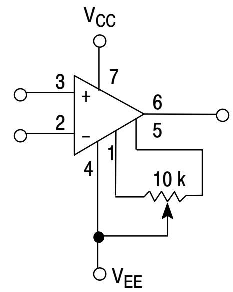


Figure 12. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply



Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171 only.

Figure 13. Offset Nulling Circuit

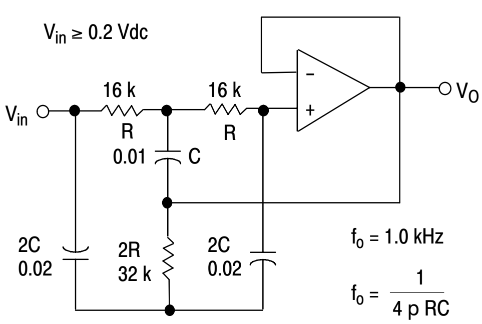
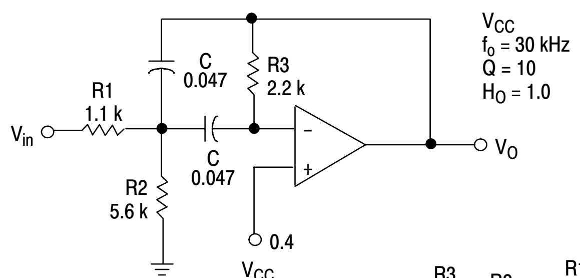


Figure 14. Active High−Q Notch Filter



Then: $R1 = \frac{R3}{2 H_O}$ $R2 = \frac{R1\ R3}{4Q^2 R1 - R3}$

$R3 = \frac{Q}{\pi f_o C}$ $\frac{Q_o\ f_o}{GBW} < 0.1$

Given f_o = center frequency
A_o = Gain at center frequency
Choose Value f_o, Q, A_o, C
For less than 10% error for operational amplifier, where f_o and GBW are expressed in Hz.

Figure 15. Active Bandpass Filter

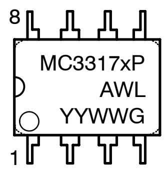
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC33171D	T_A = −40° to +85°C	SO−8	98 Units/Rail
	MC33171DG		SO−8 (Pb−Free)	
	MC33171DR2		SO−8	2500 / Tape & Reel
	MC33171DR2G		SO−8 (Pb−Free)	
	MC33171P		Plastic DIP	50 Units/Rail
	MC33171PG		Plastic DIP (Pb−Free)	
Dual	MC33172D	T_A = −40° to +85°C	SO−8	98 Units/Rail
	MC33172DG		SO−8 (Pb−Free)	
	MC33172DR2		SO−8	2500 / Tape & Reel
	MC33172DR2G		SO−8 (Pb−Free)	
	MC33172P		Plastic DIP	50 Units/Rail
	MC33172PG		Plastic DIP (Pb−Free)	
	MC33172VD	T_A = −40° to +125°C	SO−8	98 Units/Rail
	MC33172VDG		SO−8 (Pb−Free)	
	MC33172VDR2		SO−8	2500 / Tape & Reel
	MC33172VDR2G		SO−8 (Pb−Free)	
	NCV33172DR2**		SO−8	2500 / Tape & Reel
Quad	MC33174D	T_A = −40° to +85°C	SO−14	55 Units/Rail
	MC33174DG		SO−14 (Pb−Free)	
	MC33174DR2		SO−14	2500 / Tape & Reel
	MC33174DR2G		SO−14 (Pb−Free)	
	MC33174DTB		TSSOP−14*	96 Units/Rail
	MC33174DTBG		TSSOP−14*	
	MC33174DTBR2		TSSOP−14*	2500 / Tape & Reel
	MC33174DTBR2G		TSSOP−14*	
	MC33174P		Plastic DIP	25 Units/Rail
	MC33174PG		Plastic DIP (Pb−Free)	
	MC33174VDR2	T_A = −40° to +125°C	SO−14	2500 / Tape & Reel
	MC33174VDR2G		SO−14 (Pb−Free)	
	MC33174VP		Plastic DIP	25 Units/Rail
	MC33174VPG		Plastic DIP (Pb−Free)	

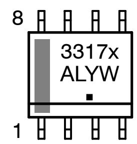
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.
**NCV prefix for automotive and other applications requiring site and control changes.

MARKING DIAGRAMS

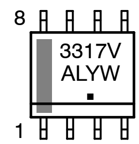
PDIP−8
P SUFFIX
CASE 626



SO−8
D SUFFIX
CASE 751



SO−8
MC33172VD
NCV33172D
CASE 751



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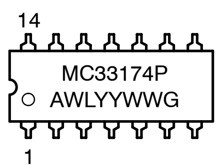
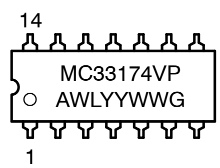
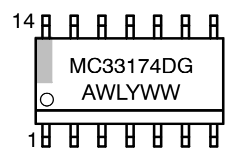
P SUFFIX
CASE 646



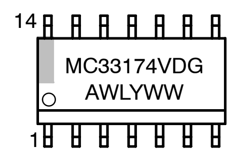
PDIP−14
VP SUFFIX
CASE 646



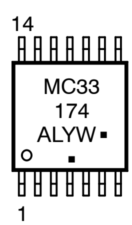
SO−14
D SUFFIX
CASE 751A



SO−14
VD SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

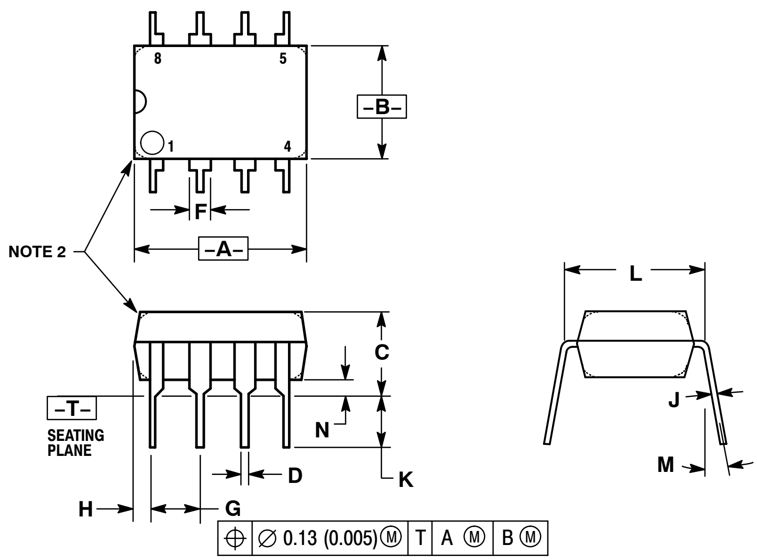


x	= 1 or 2
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L

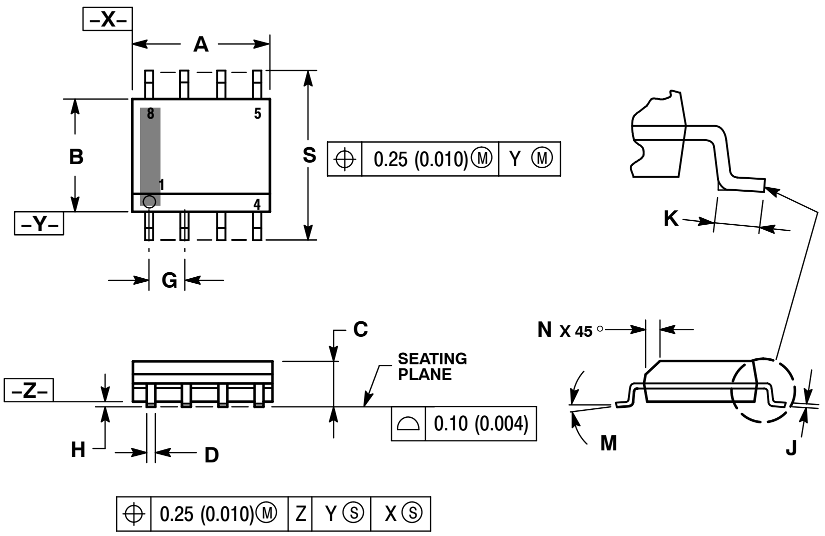


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

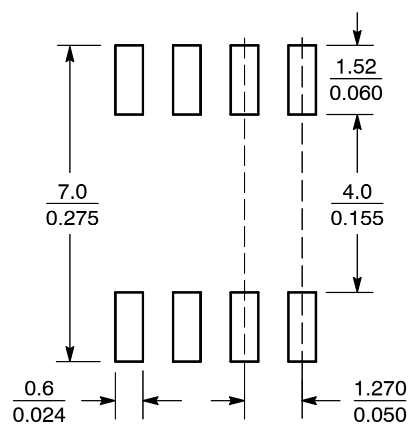
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

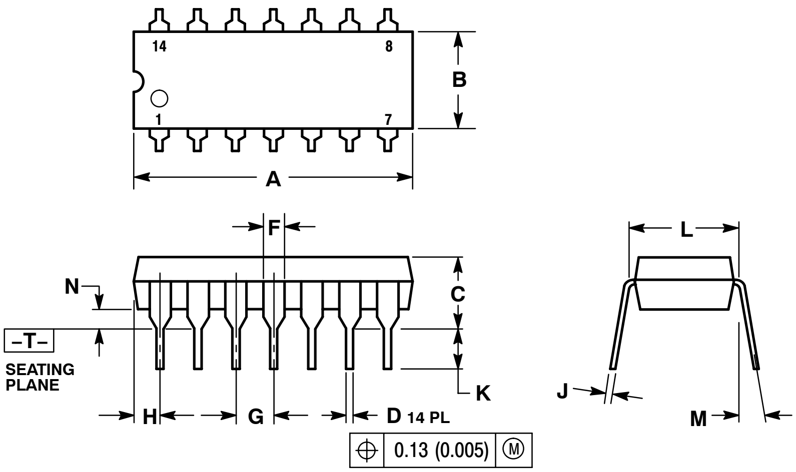


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P

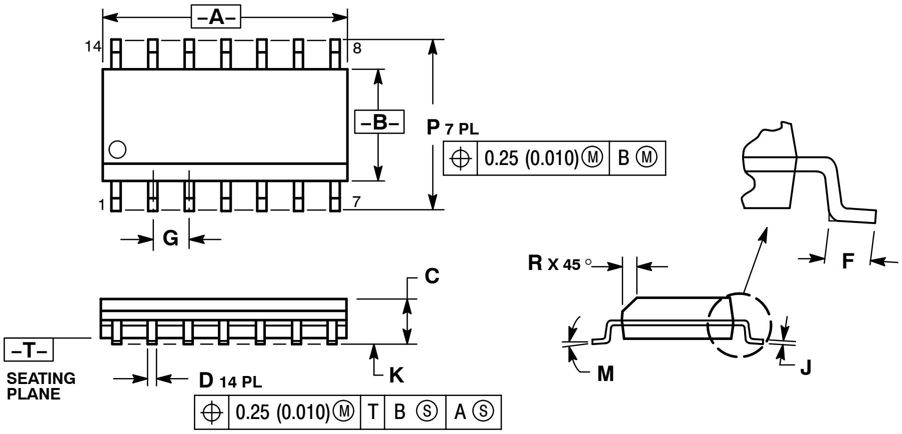


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

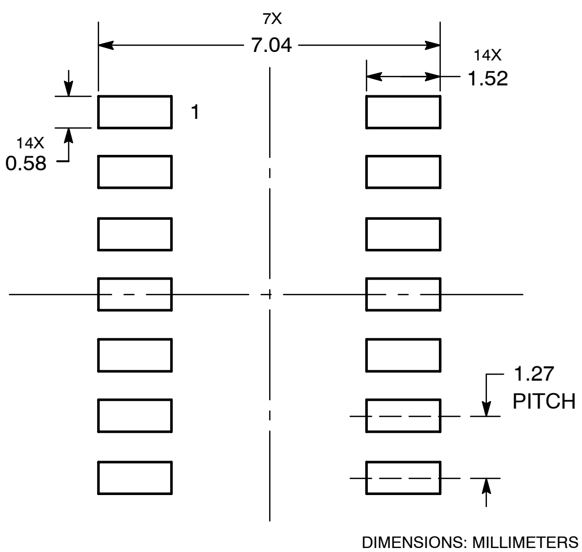
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



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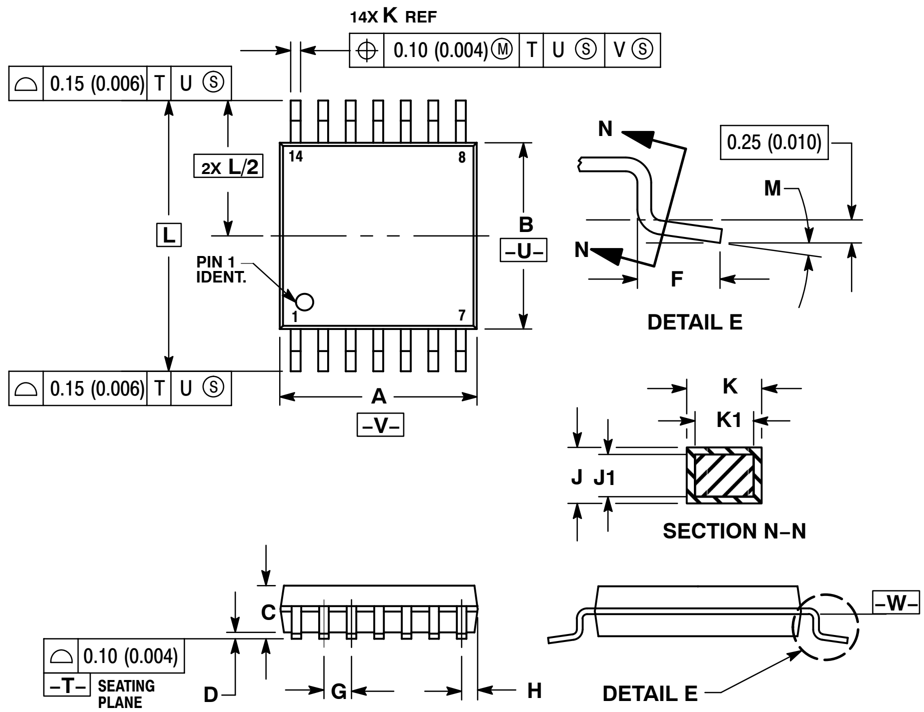
PACKAGE DIMENSIONS

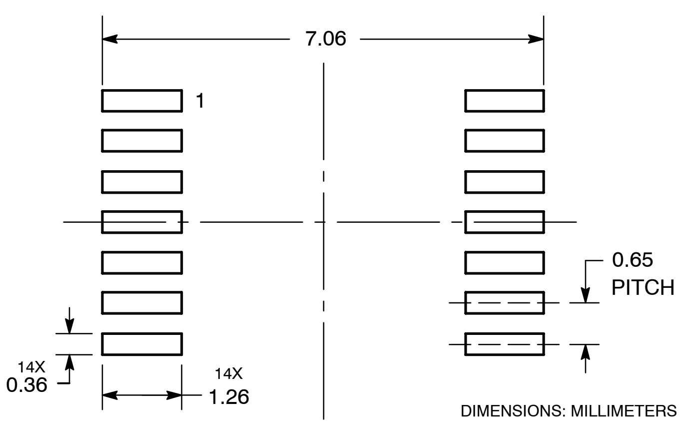
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



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